Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (currently amended): A method for debugging a system-on-a chip (SoC), the SoC comprising system components to include at least ~~one~~ a first and a second functional block, ~~each of said blocks being controlled by a block clock and a clock control unit~~, said first function block being controlled by a first block clock and a first clock control unit and said second function block being controlled by a second block clock and a second clock control unit, the method comprising ~~the~~ steps of:

setting a first breakpoint on a first specific event occurring on said first functional block ~~on the SoC~~;

monitoring events occurring on the SoC;

recognizing ~~the~~ occurrence of the first specific event on said first functional block;

providing, responsive to said recognizing, a debug trigger signal to ~~each of said~~ both said first and second clock control units;

halting, responsive to said debug trigger signal, ~~each~~ both said first and second block ~~clock~~ clocks;

determining states of one or more of said system components using a scan clock; and,

utilizing said states to debug the SoC.

Claim 2 (currently amended): The method of claim 1 in which the first specific event is an instruction that occurs ~~within a~~ within said first functional block and further comprising setting a second breakpoint on a second specific event occurring on said second functional block and wherein recognizing further comprises recognizing occurrence of the second specific event on said second functional block;

Claim 3 (currently amended): The method of claim 2 further comprising ~~the~~ step of generating a debug ready signal indicating to a user that ~~the~~ an internal state of the SoC can be observed.

Claim 4 (currently amended): The method of claim 3 wherein at least one of said first and second functional blocks comprises at least one scan chain, and said determining step comprises the steps of:

selecting from said at least one scan chain, a selected scan chain containing at least one register element;

configuring each of the at least one ~~registers~~ register element in said selected scan chain to contents required for scan mode;

~~providing control of the selected scan chain to a scan clock signal~~

providing a scan clock signal to control the selected scan chain; and,

shifting out the contents of said at least one register element in the selected scan chain.

Claim 5 (currently amended): The method of claim 1 further comprising ~~the~~ steps of:

recognizing a debug clear signal triggered by the system ~~environment~~ components and

restoring operation of each block clock.

Claim 6 (currently amended): The method of claim 1 wherein said first clock control circuit further comprises a first run counter and a first wait counter and said second clock control circuit further comprises a second run counter and a second wait counter and ~~further~~ comprising ~~the~~ steps of:

performing a single step execution of the SoC using said first and second wait counters to add delays to allow timing alignment of said first and second functional blocks; and,

redetermining the states of said one or more of said system components.

Claim 7 (currently amended): The method of ~~claim 1~~ claim 6 further comprising ~~the~~ steps of:

performing an n-cycle step execution of the SoC where n is a positive integer; and,

redetermining the states of said one or more of said system components after execution of one or more of said n-cycle steps.

Claim 8 (currently amended): The method of claim 7 wherein at least one of said functional blocks comprises at least one scan chain, and said determining step comprises ~~the~~ steps of:

selecting from said at least one scan chain, a selected scan chain containing at least one register element;

configuring each of the at least one register ~~elements~~ element in said selected scan chain to contents required for scan mode;

providing control of the scan chain to a scan clock signal; and,

shifting out the contents of the at least one register element in the selected scan chain.

Claim 9 (Canceled).

Claim 10 (currently amended): The method of ~~claim 1~~ claim 6 further comprising ~~the~~ steps of:

performing an n-cycle step execution of only one block where n is a positive integer; and,

redetermining the states of said one or more of said system components after execution of one or more of said n-cycle steps.

Claim 11 (currently amended): An apparatus for debugging a system-on-a chip (SoC), the SoC comprising system components to include at least ~~one~~ a first and a second functional block, ~~each of said functional blocks being controlled by a block clock and a clock control unit~~ said first function block being controlled by a first block clock and a first clock control unit and said second function block being controlled by a second block clock and a second clock control, the apparatus comprising:

a first controller that recognizes a first specific event occurring on said first functional block ~~the SoC~~;

a second controller that, responsive to said recognition of said first specific event, provides a debug trigger signal to ~~each of~~ said first and second clock control units;

a third controller that halts ~~each~~ said first and second block ~~clock~~ clocks upon detection of the presence of the debug trigger signal; and,

a circuit that outputs states of one or more of said system components using a scan clock;

wherein said states are utilized to debug the SoC.

Claim 12 (currently amended): The apparatus of claim 11 in which the first specific event is an instruction that occurs ~~within a~~ within said first functional block and wherein said first controller further recognizes a second specific event occurring on said second functional block and wherein said second controller provides said debug signal responsive to recognition of both said first and second specific events;

Claim 13 (original): The apparatus of claim 12 further comprising a circuit that generates a debug ready signal indicating to a user that an internal state of the SoC can be observed.

Claim 14 (currently amended): The apparatus of claim 13 wherein at least one of said functional blocks comprises at least one scan chain, and said circuit that outputs states comprises:

a circuit that selects from said at least one scan chain, a selected scan chain containing at least one register element;

a circuit that configures each of the at least one register elements in said selected scan chain to contents required for scan mode;

a circuit that provides a scan clock signal to control the selected scan chain; and,

a circuit that shifts out the contents of said at least one register element in the selected scan chain.

Claim 15 (currently amended): The apparatus of claim 11 further comprising:

a circuit that recognizes a debug clear signal triggered by the system componants ~~environment~~; and,

a circuit that restores operation of each block clock.

Claim 16 (currently amended): The apparatus of claim 11 wherein said first clock control circuit further comprises a first run counter and a first wait counter and said second clock control circuit further comprises a second run counter and a second wait counter further and further comprises a step circuit that-performs a single step execution of the SoC using said

first and second wait counters to add delays to allow timing alignment of said first and second functional blocks.

Claim 17 (currently amended): The apparatus of claim 16 wherein ~~claim 11 further comprising:~~

~~a circuit that~~ said step circuit performs an n-cycle step execution of the SoC, where n is a positive integer; and,

said circuit that outputs states comprises a circuit that re-outputs the states of said one or more of said system components after execution of one or more of said n-cycle steps.

Claim 18 (currently amended): The apparatus of claim 17 wherein at least one of said functional blocks comprises at least one scan chain, and said circuit that outputs states further comprises:

a circuit that selects from said at least one scan chain, a selected scan chain containing at least one register element;

a circuit that configures each of the at least one register ~~elements~~ element in said selected scan chain to contents required for scan mode;

a circuit that provides a scan clock signal to control the selected scan chain; and,

a circuit that shifts out the contents of said at least one register element in the selected scan chain.

Claim 19 (original): The apparatus of claim 11 further comprising:

said first controller recognizes an additional specific event occurring on the SoC;

wherein only if a predetermined condition is met with respect to said specific event and said additional specific event, does the operation of each of said second controller, said third controller and said circuit that outputs states occur.

Claim 20 (currently amended): The apparatus of claim 11 further comprising:

a circuit that performs an n-cycle step execution of only one of said functional blocks ~~block,~~ where n is a positive integer; and,

said circuit that outputs states comprises a circuit that re-outputs the states of said one or more of said system components after execution of one or more of said n-cycle steps.